



Packet No. A-67736-1/MSS/TJH  
Dorsey Matter No.: 463035-19

08/10/13  
#52  
(H)

CERTIFICATION UNDER 37 C.F.R. 1.10

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231 on March 31, 2003.

Signed:

Laura Lee Mosier

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:  
SAVAGE *et al.*

Examiner: FOX, Charles A.

Application No. 09/767,659  
Filed: January 22, 2001

Art Unit: 3652

For: Semiconductor Wafer Processing  
System with Vertically-Stacked  
Process Chambers and Single-Axis  
Dual Wafer Transfer System

Date: March 31, 2003

**AMENDMENT AFTER FINAL**

Box AF  
Assistant Commissioner for Patents  
Washington, D.C. 20231

RECEIVED  
APR 09 2003  
GROUP 3600

Sir:

This Amendment is responsive to the final Office Action mailed December 31, 2002.

Please amend the application as follows:

In the Claims:

Please amend claims 19 and 24 to read as shown:

19. (Amended) A method of semiconductor wafer processing comprising the steps of:  
providing a multi-chamber module including a plurality of vertically-stacked  
semiconductor wafer process chambers;

providing a loadlock chamber for each of the vertically-stacked semiconductor wafer  
process chambers, wherein each loadlock chamber having a transfer arm including an upper  
wafer shelf for carrying unprocessed wafers and a lower wafer shelf for carrying processed  
wafers, and a semiconductor wafer process chamber;